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(54) CLOCK RATE CONVERSION CIRCUIT

(57)Abstract:

PURPOSE: To enable clock rate conversion at an arbitrary clock frequency ratio and to realize the circuit suitable for circuit integration with a circuit configuration of simple logic.

CONSTITUTION: A DFF 14 latches a lst clock CK 1 based on a 3rd clock CK 3 having a frequency f3 being a multiple of a positive integer (N) of a frequency f2 of a 2nd clock CK 2. ADFF 13 latches an input signal sampled by the clock CK 1 by using an output of the DFF 14 as a clock signal. An output of the DFF 13 is fed to a DFF 17 via an LPF 16 operated by the clock CK 3. A 1/N frequency divider 18 is used to convert the clock CK 3 into the clock CK 2. Thec lock CK 2 is fed to the DFF 17, an output of the LPF 16 is thinned to be made 1/N from which an output signal whose frequency is converted into the frequency f2 is obtained.

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CLAIMS

[Claim(s)]

[Claim 1] It is the clock rate conversion circuit which carries out rate conversion of the input signal sampled by the 1st clock at the signal of the rate of the 2nd clock. With the 3rd clock which has a frequency twice [positive integer] (N times) the frequency of said 2nd clock The output of the 1st logical circuit which latches said 1st clock, and said 1st logical circuit is used as a clock. The 2nd logical circuit which latches said input signal, and the low pass filter with which the output of said 2nd logical circuit is supplied and which operates with said 3rd clock, The clock rate conversion circuit characterized by having supplied said 3rd clock, having thinned out the output of said low pass filter in 1-/N, and constituting from a 1-/N infanticide circuit which outputs the signal of the rate of said 2nd clock.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention aims at offering the circuit which can carry out rate conversion of the input signal in the circuitry by the easy logical circuit at the clock frequency ratio of arbitration about a clock rate conversion circuit.

[0002]

[Description of the Prior Art] For example, in signal processing of television, a Y/C separation circuit operates with a 4 times as many clock as the frequency of a chrominance subcarrier, and a scanning-line double dense circuit operates with the clock of the integral multiple of horizontal scan frequency. Thus, since the clocks of each circuit of operation differ, in order to change the clock rate of the signal to treat, the clock rate conversion circuit is used.

[0003] Moreover, also when changing two or more input signals of a different clock rate and carrying out signal processing with the same clock, the clock rate conversion circuit is used.

[0004] When changing a clock rate (sampling rate) into the signal train of a clock frequency f2 from the signal train of a clock frequency f1 and f1 and f2 are comparatively easy integer ratios, the method of performing linear interpolation is used well conventionally.

[0005] The rate conversion (the 1st conventional example) by this linear interpolation is briefly explained with drawing 4 . This drawing (A) shows the signal train x1 of a clock frequency f1, x2, x3, and --, and this drawing (B) shows the signal trains y1, y2, and y3 of a clock frequency f2, and --. In addition, let the ratio of f1 and f2 be the easy integer ratio 2:3. The signal trains y1, y2, and y3 after linear interpolation and -- become the value shown below.

[0006] y1=x1y2=(1/3) *x1 + (2/3) *x2y3=(2/3) *x2 + (1/3) It becomes the repeat of an upper type less than [*x3y4=x3y4].

[0007] However, the approach of this linear interpolation is effective only when the ratio of f1 and f2 is a comparatively easy integer ratio.

[0008] The conventional rate conversion circuit (the 2nd conventional example) in case a ratio with clock frequencies f1 and f2 is not a comparatively easy integer ratio is shown in drawing 5 . The signal train X of the rate of a clock CK 11 is inputted into a terminal 1, and is changed into an analog signal by D/A converter 2. Furthermore, the signal removed in harmonic content with the low pass filter (LPF) 3 is again changed into a digital signal by A/D converter 4 at the rate of a clock CK 22. In this case, the relation of the frequency ratio of CK11 and CK22 is free, and good.

[0009]

[Problem(s) to be Solved by the Invention] Since the 1st conventional example mentioned above was restricted when a ratio with the clock frequencies f1 and f2 before and behind conversion was a comparatively easy integer ratio, it was user-unfriendly.

[0010] As for the 2nd conventional example, D/A converter 2, LPF3, and A/D converter 4 are needed at every rate conversion. Therefore, when it constitutes a clock rate conversion circuit in the circuit of LSI, it is accompanied by the increment in an input/output terminal, and the increment in the number of LSI external components. Moreover, even if it can build in an A/D converter and a D/A converter in LSI, a chip size increases from the usual logic. A large next door and cost also increase [the above-mentioned fault], so that especially the number of clock rate conversion circuits increases.

[0011] This invention removes the conventional fault, it is circuitry by simple logic, and it aims at offering the suitable clock rate conversion circuit for IC-izing while it enables rate conversion by the clock frequency ratio of arbitration.

[0012]

[Means for Solving the Problem] In order to solve the above-mentioned technical problem then, this invention It is the clock rate conversion circuit which carries out rate conversion of the input signal sampled by the 1st clock at the signal of the rate of the 2nd clock. With the 3rd clock which has a

frequency twice [positive integer] (N times) the frequency of said 2nd clock The output of the 1st logical circuit which latches said 1st clock, and said 1st logical circuit is used as a clock. The 2nd logical circuit which latches said input signal, and the low pass filter with which the output of said 2nd logical circuit is supplied and which operates with said 3rd clock, Said 3rd clock is supplied, the output of said low pass filter is thinned out in 1-/N, and the rate conversion circuit characterized by constituting from a 1-/N infanticide circuit which outputs the signal of the rate of said 2nd clock is offered.

[0013]

[Example] The configuration of one example is illustrated to drawing 1 , and the contents are explained below. 12- 15 and 17 are D flip-flops (following, DFF), respectively. In DFF 12, 13, 15, and 17, the data inputted into each terminal D are latched with the clock inputted into each terminal CK, and are outputted from each terminal Q. DFF14 is the same as said DFF, except that the data reversed for Terminal Q are outputted.

[0014] The input signal train IN (signal sampled by the 1st clock CK 1) which carried out Iriki to the terminal 10 is supplied to the terminal D of DFF12. The output of DFF12 is supplied to the terminal D of DFF13 (the 2nd logical circuit), the output of DFF13 is supplied to the terminal D of DFF15, and the output of DFF15 is supplied to LPF16. The output of LPF16 is supplied to the terminal D of DFF17, and the output of DFF17 is outputted outside from a terminal 19 as an output signal (OUT).

[0015] On the other hand, input-clock CK1 (the 1st clock) which carried out Iriki to the terminal 11 is supplied to the terminal D of DFF14 (the 1st logical circuit) while it is supplied to the terminal CK of DFF12. The output of DFF14 is supplied to the terminal CK of DFF13. The clock CK 3 (the 3rd clock) which carried out Iriki to the terminal 20 is supplied to the 1-/N circuit 18 while it is supplied to CK terminal of DFF 14 and 15 and LPF16. The output of the 1-/N counting-down circuit 18 is supplied to a terminal 21 while it is supplied to CK terminal of DFF17. DFF17 and the 1-/N counting-down circuit 18 accomplish a 1-/N infanticide circuit.

[0016] The frequency of a clock CK 3 is set up by N times (positive integer twice) the clock CK 2 (the 2nd clock), and is twice [more than] the frequency

of CK1 further at least.

[0017] An example of the signal in each point (A) in the input signal (IN) trains D0, D1, D2, and D3 and drawing 1 to --, (D), (B), and (C) and the timing of clocks CK1 and CK3 is shown in drawing 2 . In addition, all DFF(s) shown in drawing 1 shall operate by the rising edge of the clock inputted.

[0018] (D) In the clock waveform of a point, the part which does not become settled on H or L level as shown in the slash of drawing 2 (D) arises. In actuation of DFF14, the setup time and the hold time of level of CK1 produce this, when it cannot fully secure to the rising edge of CK3.

[0019] On the other hand, a hold time becomes beyond the value which subtracted the period of CK3 from the period of L level of CK1 beyond the value to which the setup time of the data of the (A) point over the rising edge of the (D) point subtracted the period of CK3 from the period of H level of CK1. Therefore, as for DFF13, setup time and a hold time are always fully secured.

[0020] Here, if a delay period until output data start change from the rising edge of the clock inputted into DFF is set to d, a hold time will become the twice as many value of d as this to the value to which the setup time of the data of the (B) point over the rising edge of CK3 subtracted twice as many d as this from the period of CK3. Therefore, setup time and a hold time are always fully secured also for DFF15.

[0021] Input data IN is changed into the data (signal of the (C) point in drawing 1) shown in drawing 2 (C) by rate conversion by asynchronous CK1 and asynchronous CK3. The part shown with a slash is D1 or D2. It becomes an indefinite value. This is because the setup time of CK1 and a hold time are not secured to CK3 in actuation of DFF14 as it mentioned above. This phenomenon will produce a kind of phase distortion, and the spectrum of an unnecessary higher harmonic will generate it.

[0022] Drawing 3 is drawing having shown the above-mentioned phenomenon (phenomenon of spectrum generating of an unnecessary higher harmonic) with frequency spectrum.

[0023] Drawing 3 (a) shows an example of the signal train x1 of an input signal IN (sampling frequency f1), x2, and the spectrum of --. Drawing 3 (b) is the spectrum of the signal of the (C) point shown in drawing 1 , and is the

spectrum of the signal changed into the clock frequency f3 (sampling frequency of CK3). In drawing 3 (b), the parts shown with the slash between 0-f3 are the harmonic content (the first order hold of the data is carried out, and the amplitude becomes small) of the integral multiple of the frequency f1 shown in drawing 3 (a), and unnecessary harmonic content which originates in the phase fluctuation mentioned above and is generated.

[0024] Drawing 3 (c) is an example of the frequency characteristics of LPF16. With this property, the output of LPF16 serves as a signal with which the shadow area of drawing 3 (b) was removed. The output of LPF16 is latched by DFF17 and outputted to a terminal 19. However, since the clock of the frequency of f3/N (N is a positive integer) is inputted into CK terminal of DFF17 from the counting-down circuit 18, the rate of the output of DFF17 serves as f3 / N=f2. Therefore, the spectrum of the output of DFF17 is shown in drawing 3 (d).

[0025] Rate conversion of the sampling frequency is carried out from f1 by the actuation explained above at f2=f3/N, and the signal spectrum is set to (d) from drawing 3 (a) by the input signal IN by it.

[0026] Thus, although the clock rate conversion circuit of this example is simple circuitry, since the rate conversion by the clock frequency ratio of arbitration is possible for it, it is very user-friendly. Furthermore, since an A/D-conversion circuit like before, a D/A conversion circuit, LPF of an analog, and the external pin of I/O become unnecessary in LSI-izing since a simple logical circuit can constitute, and this clock rate conversion circuit can carry out [LSI]-izing on a scale of the small-scale gate, it can attain much more low-cost-izing and a miniaturization.

[0027] Next, an example of the rate conversion at the time of using this clock rate conversion circuit for a television digital disposal circuit is shown. It is as follows, when supposing that they are color-subcarrier-frequency fsc=3579545Hz and ihorizontal-synchronous-frequency fh=2/455*fsc=15734Hz and carrying out rate conversion of the sampling frequency f1=4*fsc=14.318MHz of an input signal at f2=1024*fh=16.112MHz.

[0028] The frequency f3 of a clock CK 3 will be set to f3=4*f2=64.448MHz if N in the 1-/N counting-down circuit 18 is set to 4. Moreover, if LPF16 is used as

the transversal filter of nine taps and each tap multiplier is set to (1/64, 4/64, 8/64, 12/64, 14/64, 12/64, 8/64, 4/64, and 1/64), the frequency characteristics of this LPF16 will turn into a property shown in drawing 3 (c). The band where the amplitude becomes 1/2 or more to the amplitude at the time of a frequency 0 is set to about 6.4MHz. Therefore, the spectrum of the signal by which rate conversion was carried out at f2=16.112MHz turns into a spectrum shown in drawing 3 (d) of about 6MHz of bands.

[0029] In addition, in this example, although DFF was used for the 1st and 2nd logical circuit and a 1-/N infanticide circuit, other logical circuits which can latch a signal, of course may be used.

[0030]

[Effect of the Invention] Although the clock rate conversion circuit of this invention is simple circuitry as above, since the rate conversion by the clock frequency ratio of arbitration is possible, it is very user-friendly. Furthermore, since an A/D-conversion circuit like before, a D/A conversion circuit, LPF of an analog, and the external pin of I/O become unnecessary in LSI-izing since a simple logical circuit can constitute, and this clock rate conversion circuit can carry out [LSI]-izing on a scale of the small-scale gate, it can attain much more low-cost-izing and a miniaturization.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is drawing showing the configuration of one example.

[Drawing 2] It is the timing chart of an example of operation.

[Drawing 3] It is drawing showing the signal spectrum in an example.

[Drawing 4] It is drawing for explaining the 1st conventional example.

[Drawing 5] It is drawing showing the 2nd conventional example.

[Description of Notations]

12- 15 and 17 DFF (D flip-flop)

16 LPF

18 1/N Counting-down Circuit